EN0-001 Q&As

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QUESTION 1

An advantage of removable flash memory over built-in flash memory is that:

A. Storage can be easily replaced, for example to increase capacity.

B. It is quicker to access, providing far greater bandwidth for read operations.

C. It has a longer life, indicated by being rated for a higher number of write cycles.

D. It takes up less physical space in a device, and does not require any space on the printed circuit board.

Correct Answer: A

QUESTION 2

Which of the following statements is TRUE with respect to the power consumption related to memory accesses?

A. Accessing a large memory device consumes less power than accessing a small one

B. A series of non-sequential accesses is more efficient than a series of sequential accesses

C. Increasing the size of the cache will always reduce power consumption for a given application

D. Storing frequently used data in Tightly Coupled Memory will reduce power consumption

Correct Answer: D

QUESTION 3

In an ARMv7-R processor, with which level of the memory system is the Memory Protection Unit (MPU) associated?

A. Level 1

B. Level 2

C. Level 3

D. Level 4

Correct Answer: A

QUESTION 4

In which of these cases would code have better performance when compiled for Thumb state than when compiled for ARM state?

A. When the processor has no data cache

B. When the code involves many shifting operations

C. When the code has many conditionally executed instructions

D. When the processor can only fetch instructions 16-bits at a time

Correct Answer: D

QUESTION 5

Optimizing for space will:

A. Produce an image which is decompressed at run-time.

B. Cause the compiler to unroll loops where possible.

C. Result in more functions being inlined by the compiler.

D. Produce smaller code, even if this results in slower execution.

Correct Answer: D

QUESTION 6

An interrupt handler contains the following instruction sequence at the end. The purpose of these instructions is to clear the interrupt request in the interrupt controller and then safely re-enable interrupts.

STR r0, [r1] ; write to interrupt controller register to clear interrupt request

CPSIE i ; re-enable IRQ interrupts Which of the following instructions should be placed at position in order to ensure that the interrupt

controller sees the write before interrupts are re-enabled?

A. DMB

B. DSB

C. ISB

D. NOP

Correct Answer: B

QUESTION 7

What is an "Entry point" in an application?

A. A place where execution can start

B. The location of the main () function

C. The lowest address contained in a program image

D. A location where the linker can store additional information

Correct Answer: A

QUESTION 8

The Cortex-A9 processor has 6 breakpoint units and 4 watchpoint units. What is the maximum number of breakpoints the debugger can set on code in ROM?

A. 6

B. 10

C. 2

D. The debugger can use the BKPT instruction to do this.

Correct Answer: A

QUESTION 9

On an ARM processor that does not implement Security Extensions, which one of the following can be the starting address of the exception vector table?

A. 0xFFFFFFFF

B. 0xFFFFFFF0

C. 0xFFFF0000

D. 0x0000FFFF

Correct Answer: C

QUESTION 10

An application contains three calls to an external function, foobar(), which is defined in a shared (or dynamic) library. How many copies of foobar() will the linker place in the application image?

(Ignore linker inlining)

A. None

B. Always one

C. Always three

D. One or more depending on optimization level

Correct Answer: A

QUESTION 11

What is the value of r0 after executing the following instruction sequence?

MOV r0, #200

MOV r5, #1

STR r3, [r0, r5, LSL#3]!

A. 200

B. 201

C. 204

D. 208

Correct Answer: D

QUESTION 12

The following pair of functions implement a simple mutex spinlock which might be used to protect a critical code section in a multi-threaded application. The address of the lock variable is in r0.

```
lock_mutex:
    ldrex   r1, [r0]
    cmp     r1, #LOCKED
    <A>
    beq     lock_mutex

try_lock:
    <B>
    mov     r1, #LOCKED
    strex   r2, r1, [r0]
    cmp     r2, #0
    bne     lock_mutex
    dmb
    bx      lr

unlock_mutex:
    dmb
    <C>
    mov     r1, #UNLOCKED
    str     r1, [r0]
    dsb
    <D>
    bx      lr
```

In order to minimize power while waiting for the lock to be available. SEV and WFE instructions can be used to place the processor in a low power state while waiting for the lock to become available. At which points should these instructions be placed?

A. WFENE at , SEV at

B. WFEEQ at SEV at

C. WFE at **SEV at WFENE at**

D. SEV at

Correct Answer: B

QUESTION 13

Which of the following instructions can be used to enter a power saving mode?

A. PLD

B. PLI

C. WFE

D. DSB

Correct Answer: C

QUESTION 14

An ARM Cortex-A9 multi-core system has two CPUs, C1 and C2, each with a corresponding data cache. The code running on C1 writes to a memory location M. and C1 updates its data cache, but not main memory. After that, C2 tries to read the contents of memory location M. Which of the following hardware can automatically (without software inteivention) ensure that C2 reads the updated contents of M?

A. Snoop Control Unit

B. Tightly Coupled Memory

C. Level 2 Cache Controller

D. Dynamic Memory Access Controller

Correct Answer: A

QUESTION 15

A re-entrant interrupt handler would typically be used to:

A. Allow an external interrupt to interrupt an SVC handler

B. Reduce response time for higher priority interrupts

C. Allow an interrupt handler to be relocated in memory

D. Avoid the need for an interrupt handler to use a stack.

Correct Answer: B