EN0-001 Q&As

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QUESTION 1

What type of instruction is used for cache maintenance operations?

A. Dedicated ARM instructions

B. Dedicated Thumb instructions

C. CP14 instructions

D. CP15 instructions

Correct Answer: D

QUESTION 2

A function written in C has the prototype:

void my_function(float a. double b, float c);

The function is built and linked into an application using hard floating-point linkage. What registers are

used to pass arguments to the function?

A. a->s0; b->d0; c->s1

B. a->s0; b->d1; c->s1

C. a->d0; b->d1; c->d2

D. a->s0; b->d1; c-> s2

Correct Answer: B

QUESTION 3

When using a Generic Interrupt Controller (GIC), how does code cause a software-generated interrupt?

A. By executing an SGI instruction

B. By writing to a register in the GIC

C. By writing to the F bit in the CPSR

D. By writing to the I bit in the CPSR

Correct Answer: B

QUESTION 4

In an operating system environment, most applications are executed in which processor mode?

A. Supervisor

B. IRQ

C. System

D. User

Correct Answer: D

QUESTION 5

Assuming a 4-core Cortex-A9 SMP system which does not use the Accelerator Coherency Port (ACP). and operates the L1 caches in writeback mode, in which of the following situations is a cache clean operation required?

A. An external DMA engine modifies data in a region of data memory which is already cached by the processor

B. An external agent needs to read data which has been modified by the processor in a cacheable memory region

C. Debugger reads data from a shared, cacheable memory location

D. One core modifies data in a shared cacheable memory region

Correct Answer: B