

# **EN0-001** Q&As

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#### **QUESTION 1**

Which of these instructions is a correct translation of the body of function f?

struct T { char a; int b; };

int f(struct T \*p) { return p->b; }

A. LDR r0, [r0], #1

B. LDR r0, [r0]. #4

C. LDR r0, [r0.#1]

D. LDR r0, [r0. #4]
Correct Answer: D

#### **QUESTION 2**

A deeply embedded real-time industrial control system is missing some hard real-time interrupt deadlines. Which of the following performance analysis techniques is the most suitable for identifying which routines are causing the problem?

- A. Use an ETM instruction trace profiler, which outputs information about the program as it runs
- B. Add some serial logging to the software, which outputs information about the program as it runs
- C. Add a new interrupt handler, which is triggered off a timer, and dump information about the interrupted process
- D. Use a JTAG sample-based profiler, which periodically halts the CPU, and dumps information about the interrupted process

Correct Answer: A

#### **QUESTION 3**

When using an Operating System, which instruction is used by user code to request a service from the kernel?

A. BLX

B. RFEFD

C. SRSFD

D. SVC

Correct Answer: D

## QUESTION 4



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When the processor is executing in Thumb state, which of the following statements is correct about the values stored in R15?

- A. Bits[31:16] are duplicated with bits[15:0]
- B. The PC value is stored in bits[31:1] and bit[0] is treated as zero
- C. The PC value is stored in bits[31:16] and bits[15:0] are undefined
- D. The PC value is stored in bits[15:0] and bits[31:16] are undefined

Correct Answer: B

#### **QUESTION 5**

What type of instruction is used for cache maintenance operations?

- A. Dedicated ARM instructions
- B. Dedicated Thumb instructions
- C. CP14 instructions
- D. CP15 instructions

Correct Answer: D

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