EN0-001 Q&As

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QUESTION 1

Why does Device memory prohibit speculative accesses?

A. Speculative accesses might waste energy

B. Speculative accesses might reduce performance

C. Speculative accesses might cause unwanted cache coherency traffic

D. Speculative accesses might cause undesired system state changes

Correct Answer: D

QUESTION 2

Processors which implement the ARMv7-A architecture can be configured to allow unaligned memory access. Unaligned accesses have a number of advantages, disadvantages, and limitations.

Which TWO of the following statements are true? (Choose two)

A. Unaligned accesses may take more cycles to execute than aligned accesses

B. Unaligned loads and stores are necessary for accessing fields in packed structures

C. A program compiled using unaligned accesses can be safely executed on all ARMv7-A devices

D. If the relevant control register setting is enabled all loads and stores can function from unaligned addresses

E. Unaligned accesses can only be made to Normal memory

Correct Answer: AE

QUESTION 3

Consider the following code sequence, executing on a processor which implements ARM Architecture v7

A.

LDR r0, [r1]

STR r0, [r2]

STR r3, [r3]

R1 points to a location in normal memory. R2 and R3 point to device memory.

Which of the following statements best describes the ordering rules which apply to this sequence?

A. The two writes to device memory will happen in program order, but the read can be performed out of order

B. The memory accesses can happen in any order

C. The memory accesses will happen in program order

D. The read to r0 and the write from r0 will happen in program order, but the write from r3 can be performed out of order

Correct Answer: C

QUESTION 4

Assuming a 4-core Cortex-A9 SMP system which does not use the Accelerator Coherency Port (ACP). and operates the L1 caches in writeback mode, in which of the following situations is a cache clean operation required?

A. An external DMA engine modifies data in a region of data memory which is already cached by the processor

B. An external agent needs to read data which has been modified by the processor in a cacheable memory region

C. Debugger reads data from a shared, cacheable memory location

D. One core modifies data in a shared cacheable memory region

Correct Answer: B

QUESTION 5

Which of the following processor resources do NOT have to be saved or modified by the Linux scheduler during context switch?

A. Registers R0-R15

B. Thread and process ID registers

C. The CPSR

D. NEON and VFP registers

Correct Answer: D