

EN0-001 Q&As

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QUESTION 1

Which instruction would be used to return from a Reset exception?

A. MOVS PC, R14

- B. MOVSPC, R13
- C. Architecturally not defined
- D. SUBS PC, R14, #4

Correct Answer: C

QUESTION 2

When building code for both ARM and Thumb states, which tool decides for each function call whether to use a BL or BLX instruction?

- A. The linker
- B. The archiver
- C. The compiler
- D. The assembler
- Correct Answer: A

QUESTION 3

If the processor is in User mode and then an IRQ interrupt occurs:

- A. CPSR mode bits are set to User mode and SPSR _User mode bits are set to IRQ.
- B. CPSR mode bits are set to IRQ and SPSR_Irq mode bits are set to User.
- C. CPSR mode bits are set to IRQ and SPSR_Irq mode bits are set to IRQ.
- D. CPSR mode bits are set to User and SPSR User mode bits are set to IRQ.

Correct Answer: B

QUESTION 4

What side-effect could using a debugger to read memory contents have?

A. The memory contents could be set to zero



- B. Some memory contents could be rewritten
- C. The processor MMU pagetables could be modified
- D. The processor cache could be cleaned or/and invalidated

Correct Answer: D

QUESTION 5

In which of the following scenarios would cache maintenance operations be necessary in an ARMv7 system?

- A. Before executing code that uses the NEON instruction set
- B. Before handling an interrupt request raised by an external device
- C. Before checking the status of a semaphore
- D. Before reading cacheable memory that has been written to by an external bus master

Correct Answer: D

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