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QUESTION 1

What architecture does the ARM11 MPCore implement?

A. ARMv6

B. ARMv6K

C. ARMv7-A

D. ARMv7-A with the Multiprocessing Extensions

Correct Answer: B

QUESTION 2

LDREX and STREX were introduced in which ARM architecture version?

A. ARMv5TE

B. ARMv6

C. ARMv6K

D. ARMv7

Correct Answer: B

QUESTION 3

Under which of the following data-sharing scenarios would cache maintenance operations be necessary?

A. Sharing data with another thread running on the same core

B. Sharing data with another process running on the same core

C. Sharing data with an external device

D. Sharing data with another CPU in an SMP system

Correct Answer: C

QUESTION 4

An ARMv7 implementation might include the VFPv4-D32 floating point extension. What does the \\'32\\' indicate?

A. The width of the datapath in bits

B. The number of double precision floating point registers implemented

C. The number of bits of data that can be loaded or stored at once

D. The number of integer operations that can be performed simultaneously

Correct Answer: B

QUESTION 5

In an ARMv7-A processor that includes the Advanced SIMD extension (NEON), where are the data values operated on by NEON instructions stored?

A. In system memory

B. In registers shared with the VFP register set

C. In registers shared with the integer register set

D. In dedicated registers not shared with other registers

Correct Answer: B

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